This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (currently amended): A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

a plurality of lead lines for connecting the gate electrodes to an external circuit and a plurality of connection terminals for connecting the gate electrodes to the external circuit,

the gate electrodes making up N of gate electrode groups in which the lines belonging to each coset of modulo N within successive pixel rows are connected to common lead lines, N being a predetermined natural number between 4 and one half the number of pixels in a column, and N also being the minimum periodic unit of connections from said gate electrodes <u>having the same modulo N value and belonging to different gate electrode groups</u> to said connection terminals within said successive pixel rows, the gate ~~electrodes~~ <u>electrode groups</u> having common connection terminals to

(i) reduce the number of the connection terminals to less than N, and

(ii) enable the gate electrodes having common connection terminals to be controlled with different timing from the timing of non-common connection terminals of the gate electrode groups.

Claim 2 (currently amended): A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

a plurality of lead lines for connecting the gate electrodes to an external circuit and a plurality of connection terminals for connecting the gate electrodes to the external circuit,

gate control lines connected to gate electrode groups in which horizontal lines belonging to each coset of modulo N within successive pixel rows are connected commonly, N being a predetermined natural number between 4 and one half the number of pixels in a column, and N also being the minimum periodic unit of connections from said gate electrodes <u>having the same modulo N value and belonging to</u>

different gate electrode groups to said connection terminals within said successive pixel rows, being combined with each other so as to

(i) reduce the number of the connection terminals to less than N, and

(ii) enable the gate electrodes having common connection terminals to be controlled with different timing from the timing of non-common connection terminals of the gate electrode groups.

Claim 3 (currently amended): A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

a plurality of lead lines for connecting the gate electrodes to an external circuit and a plurality of connection terminals for connecting the gate electrodes to the external circuit,

the gate electrodes being provided in a predetermined number N of gate electrode groups such that horizontal line number of the gate electrode groups which are connected to respective common lead lines belong to each same residue

class of modulo N, N being a predetermined natural number between 4 and one half the number of pixels in a column, and N also being the minimum periodic unit of connections from said gate electrodes having the same modulo N value and belonging to different gate electrode groups to said connection terminals within said successive pixel rows, some of the gate electrode groups being commonly connected

(i) so that the connection terminals are less in number than N, and

(ii) to enable the gate electrodes having common connection terminals to be controlled with different timing from the timing of non-common connection terminals of the gate electrode groups.

Claim 4 (currently amended): A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

a plurality of lead lines for connecting the gate electrodes to an external circuit and a plurality of connection terminals for connecting the gate electrodes to the external circuit,

the gate electrodes making up N of gate electrode groups in which the lines belonging to each coset of modulo N within successive pixel rows are connected to common lead lines, N being a predetermined natural number between 4 and one half the number of pixels in a column, and N also being the minimum periodic unit of connections from said gate electrodes <u>having the same modulo N value and belonging to different gate electrode groups</u> to said connection terminals within said successive pixel rows, the gate electrode groups having common connections to

(i) reduce the number of the connection terminals to less than N, and

(ii) enable the gate electrodes having common connection terminals to be controlled with different timing from the timing of non-common connection terminals of the gate electrode groups,

wherein the commonly connected gate electrode groups are always controlled in the same way in each of all predetermined read-out modes including selective pixel read-out modes by selective shift gate driving.

Claim 5 (currently amended): A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

a plurality of lead lines for connecting the gate electrodes to an external circuit and a plurality of connection terminals for connecting the gate electrodes to the external circuit,

gate control lines connected to gate electrode groups in which the horizontal lines belonging to each coset of modulo N within successive pixel rows are connected commonly, N being a predetermined natural number between 4 and one half the number of pixels in a column, and N also being the minimum periodic unit of connections from said gate electrodes <u>having the same modulo N value and belonging to different gate electrode groups</u> to said connection terminals within said successive pixel rows, being combined with each other so as to

(i) reduce the number of the connection terminals to less than N, and

(ii) enable the gate electrodes having common connection terminals to be controlled with different timing from the timing of non-common connection terminals of the gate electrode groups,

wherein the commonly connected gate electrode groups are always controlled in the same way in each of all predetermined read-out modes including selective pixel read-out modes by selective shift gate driving.

Claim 6 (currently amended): A solid-state imaging device comprising:

a pixel unit constituted by a two-dimensional array of pixels for generating charge in correspondence to received light and accumulating the charge for a predetermined period of time;

a vertical transfer unit for vertically transferring charge from the pixels in the pixel unit, a horizontal transfer unit for horizontally transferring charge from the vertical transfer unit;

shift gates each provided between each pixel and the vertical transfer unit for reading out the charge in the pixels to the vertical transfer unit, gate electrodes for controlling the shift gates; and

a plurality of lead lines for connecting the gate electrodes to an external circuit and a plurality of connection terminals for connecting the gate electrodes to the external circuit,

the gate electrodes being provided in a predetermined number N of gate electrode groups such that horizontal line number of the gate electrode groups which are connected to respective common lead lines belong to each same residue class of modulo N, N being a predetermined natural number between 4 and one half the number of pixels in a column, and N also being the minimum periodic unit of connections from said gate electrodes <u>having the same modulo N value and belonging to different gate electrode groups</u> to said connection terminals within said successive pixel rows, some of the gate electrode groups being commonly connected

(i) so that the connection terminals are less in number than N, and

(ii) to enable the gate electrodes having common connection terminals to be controlled with different

timing from the timing of non-common connection terminals of the gate electrode groups,

wherein the commonly connected gate electrode groups are always controlled in the same way in each of all predetermined read-out modes including selective pixel read-out modes by selective shift gate driving.

Claim 7 (previously presented): The solid-state imaging device according to claim 4, wherein gate electrode groups controlled in each of all the predetermined read-out modes are set such as to provide a minimum number of connection terminals for connecting the gate electrodes to an external circuit.

Claim 8 (previously presented): The solid-state imaging device according to claim 5 wherein gate electrode groups controlled in each of all the predetermined read-out modes are set such as to provide a minimum number of connection terminals for connecting the gate electrodes to an external circuit.

Claim 9 (previously presented): The solid-state imaging device according to claim 6 wherein gate electrode groups controlled in each of all the predetermined read-out modes are set such as to provide a minimum number of connection terminals for connecting the gate electrodes to an external circuit.

Claims 10 and 11 (canceled)

Claim 12 (previously presented): The solid-state imaging device of claim 1 wherein at least two horizontal lines

belonging to the same pixel group but to different gate electrode groups are connected to a common connection terminal.

Claim 13 (previously presented): The solid-state imaging device of claim 2 wherein at least two horizontal lines belonging to the same pixel group but to different gate electrode groups are connected to a common connection terminal.

Claim 14 (previously presented): The solid-state imaging device of claim 3 wherein at least two horizontal lines belonging to the same pixel group but to different gate electrode groups are connected to a common connection terminal.

Claim 15 (previously presented): The solid-state imaging device of claim 4 wherein at least two horizontal lines belonging to the same pixel group but to different gate electrode groups are connected to a common connection terminal.

Claim 16 (previously presented): The solid-state imaging device of claim 5 wherein at least two horizontal lines belonging to the same pixel group but to different gate electrode groups are connected to a common connection terminal.

Claim 17 (previously presented): The solid-state imaging device of claim 6 wherein at least two horizontal lines belonging to the same pixel group but to different gate electrode groups are connected to a common connection terminal.

Claim 18 (previously presented): The solid-state imaging device of claim 1 wherein only two connection terminals connected to said vertical transfer unit are not connected to any of the gate electrodes.

Claim 19 (previously presented): The solid-state imaging device of claim 2 wherein only two connection terminals connected to said vertical transfer unit are not connected to any of the gate electrodes.

Claim 20 (previously presented): The solid-state imaging device of claim 3 wherein only two connection terminals connected to said vertical transfer unit are not connected to any of the gate electrodes.

Claim 21 (previously presented): The solid-state imaging device of claim 4 wherein only two connection terminals connected to said vertical transfer unit are not connected to any of the gate electrodes.

Claim 22 (previously presented): The solid-state imaging device of claim 5 wherein only two connection terminals connected to said vertical transfer unit are not connected to any of the gate electrodes.

Claim 23 (previously presented): The solid-state imaging device of claim 6 wherein only two connection terminals connected to said vertical transfer unit are not connected to any of the gate electrodes.

Claim 24 (previously presented): The solid-state imaging device of claim 1 wherein connections from said gate

electrodes to said connection terminals within successive pixel rows have a periodic repetition, and wherein N is the minimum period of repetition.

Claim 25 (previously presented): The solid-state imaging device of claim 1 wherein connections from said gate electrodes to said connection terminals within successive pixel rows exhibit a repeating pattern, and wherein N is the minimum period of the repeating pattern.